line 14 paragraph filed July 25, 2001 was objected to as containing "at the 7th line an incorrect U.S. Application Serial No." In paragraph 3, applicants were further requested to update the incorporated applications information on pages 8 and 9. Further, in paragraph 4, applicants were reminded that references to figures should be consistent throughout the specification with particular reference to Fig. 1 or Fig. 1A on pages 6-9, 10, and 12. Each of the above items is addressed in order below. Attached hereto is a marked-up version showing the changes made to the specification and claims by the current amendment. The attached pages are captioned **Version with Markings to Show Changes Made**.

Drawing Corrections

A proposed red-lined drawing correction changing "Fig. 1" to --Fig. 1A-- is submitted for the Examiner's approval.

Paragraph 2 Objection

The typographical error in the Serial No. has been corrected by amendment and the patent number for this application has also been added.

Paragraph 3 Updating

Updating information for pages 8 and 9 has been provided. MPEP § 608.01(p) at page 600-79 states an "application for a patent when filed may incorporate "essential material" by reference to (1) a U.S. patent, (2) a U.S. patent application publication, or (3) a pending U.S. application." Nonessential subject matter can also be incorporated by reference to U.S. patents or prior filed, commonly assigned U.S. applications. There is no indication that inventor information need be provided and it is believed that this information is not necessary to properly identify the

patent or application incorporated by reference. Please call the undersigned should further information be required.

Paragraph 4 Updating

The specification has been amended to consistently refer to Fig. 1A consistent with the drawing correction.

Conclusion

All of the claims standing in order for allowance, this case should be promptly allowed. Should there be any issues which might be expedited by a telephone call, the Examiner is requested to call the undersigned at the number below.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Drawings

Red-lined proposed drawing corrections to sheet 1 of the drawings are submitted herewith for the Examiner's approval.

In the Specification

Please replace the paragraph beginning at page 6, line 1 and extending to page 7, line 19 as follows:

--In one embodiment of the present invention, a manifold array (ManArray) architecture is adapted to employ various aspects of the present invention to solve the problem of configurable application-specific instruction set optimization and program size reduction, thereby increasing code density and making the general ManArray architecture even more desirable for high-volume and portable battery-powered types of products. The present invention extends the pluggable instruction set capability of the ManArray architecture described in U.S. Application Serial No. [09/228,374] 09/215,081 filed December 18, 1998, now U.S. Patent No. 6,101,592, entitled "Methods and Apparatus for Scalable Instruction Set Architecture with Dynamic Compact Instructions" with new approaches to program code reduction and stand-alone operation using only abbreviated instructions in a manner not previously described.--

Please replace the paragraph beginning at page 8, line 9 as follows:

--Further details of a presently preferred ManArray architecture for use in conjunction with the present invention are found in U.S. Patent [Application Serial] No. [08/885,310 filed June 30, 1997] 6,023,753, U.S. Patent [Application Serial] No. [08/949,122 filed October 10,

1997] 6,167,502, U.S. Patent Application Serial No. 09/169,255 filed October 9, 1998, U.S. Patent [Application Serial] No. [09/169,256 filed October 9, 1998] 6,167,501, U.S. Patent [Application Serial] No. [09/169,072 filed October 9, 1998] 6,219,776, U.S. Patent [Application Serial] No. [09/187,539 filed November 6, 1998] 6,151,668, U.S. Patent [Application Serial] No. [09/205,558 filed December 4, 1998] 6,173,389, U.S. Patent [Application Serial] No. [09/215,081 filed December 18, 1998] 6,101,592, U.S. Patent [Application Serial] No. [09/228,374 filed January 12, 1999] 6,216,223, U.S. Patent Application Serial No. 09/238,446 filed January 28, 1999, U.S. Patent Application Serial No. 09/267,570 filed March 12, 1999, as well as, Provisional Application Serial No. 60/092,130 entitled "Methods and Apparatus for Instruction Addressing in Indirect VLIW Processors" filed July 9, 1998, Provisional Application Serial No. 60/103,712 entitled "Efficient Complex Multiplication and Fast Fourier Transform (FFT) Implementation on the ManArray" filed October 9, 1998, Provisional Application Serial No. 60/106,867 entitled "Methods and Apparatus for Improved Motion Estimation for Video Encoding" filed November 3, 1998, Provisional Application Serial No. 60/113,637 entitled "Methods and Apparatus for Providing Direct Memory Access (DMA) Engine" filed December 23, 1998, Provisional Application Serial No. 60/113,555 entitled "Methods and Apparatus Providing Transfer Control" filed December 23, 1998, Provisional Application Serial No. 60/139,946 entitled "Methods and Apparatus for Data Dependent Address Operations and Efficient Variable Length Code Decoding in a VLIW Processor" filed June 18, 1999, Provisional Application Serial No. 60/140,245 entitled "Methods and Apparatus for Generalized Event Detection and Action Specification in a Processor" filed June 21, 1999, Provisional Application Serial No. 60/140,163 entitled "Methods and Apparatus for Improved Efficiency in Pipeline Simulation and Emulation" filed June 21, 1999, Provisional Application Serial No. 60/140,162 entitled "Methods and Apparatus for Initiating and Re-Synchronizing Multi-Cycle SIMD

Instructions" filed June 21, 1999, Provisional Application Serial No. 60/140,244 entitled "Methods and Apparatus for Providing One-By-One Manifold Array (1x1 ManArray) Program Context Control" filed June 21, 1999, Provisional Application Serial No. 60/140,325 entitled "Methods and Apparatus for Establishing Port Priority Function in a VLIW Processor" filed June 21, 1999, and Provisional Application Serial No. 60/140,425 entitled "Methods and Apparatus for Parallel Processing Utilizing a Manifold Array (ManArray) Architecture and Instruction Syntax" filed June 22, 1999 respectively, all of which are assigned to the assignee of the present invention and incorporated by reference herein in their entirety.--

Please replace the paragraphs beginning at page 9, line 20 and extending to page 12, line 16 as follows:

--In a presently preferred embodiment of the present invention, a ManArray 2x2 iVLIW single instruction multiple data stream (SIMD) processor 100 as shown in Fig. 1A is used. Processor 100 comprises a sequence processor (SP) controller combined with processing element-0 (PE0) SP/PE0 101, as described in further detail in co-pending U.S. Patent Application Serial No. 09/169,072, now U.S. Patent No. 6,219,776, entitled "Methods and Apparatus for Dynamic Merging an Array Controller with an Array Processing Element" and filed October 9, 1998. Three additional PEs 151, 153, and 155 are also utilized to demonstrate the abbreviated instruction and configurable processor architecture and apparatus. Note that the PEs can be also labeled with their matrix positions as shown in parentheses for PE0 (PE00) 101, PE1 (PE01)151, PE2 (PE10) 153, and PE3 (PE11) 155. The SP/PE0 101 contains a fetch controller 103 to allow the fetching of abbreviated- instruction words from a B-bit instruction memory 105, where B is determined by the application instruction-abbreviation process to be a reduced number of bits representing ManArray native instructions and/or to contain two or more

abbreviated instructions as further described below. The fetch controller 103 provides the typical functions needed in a programmable processor, such as a program counter (PC), a branch capability, eventpoint loop operations (for further details of such operation see U.S. Provisional Application Serial No. 60/140,245 entitled "Methods and Apparatus for Generalized Event Detection and Action Specification in a Processor" filed June 21, 1999) and support for interrupts. Fetch controller 103 also provides instruction memory control which could include an instruction cache if needed by an application. The fetch controller 103 additionally provides the abbreviated-instruction translation apparatus described in the present invention. In addition, fetch controller 103 which may also be referred to as an instruction-fetch or I-fetch unit dispatches translated native instruction words and instruction control information to the other PEs in the system by means of a D-bit instruction bus 102. The D-bit instruction bus 102 may include additional control signals as needed in an abbreviated-instruction translation apparatus.

In this exemplary system 100 of Fig. 1A, common elements are used throughout to simplify the explanation, though actual implementations are not limited to this restriction. For example, the execution units 131 in the combined SP/PE0 101 can be separated into a set of execution units optimized for the control function with fixed point execution units in the SP, while PE0 as well as the other PEs can be optimized for a floating point application. For the purposes of the present description, it is assumed that the execution units 131 are of the same type in the SP/PE0 101 and the PEs 151, 152 and 153. In a similar manner, the SP/PE0 and the other PEs use a five instruction slot iVLIW architecture which contains a VLIW memory (VIM) 109 and an instruction decode and VIM controller function unit 107 which receives instructions as dispatched from the SP/PE0's I-fetch unit 103 and generates the VIM addresses and control signals 108 required to access the iVLIWs stored in the VIM. Store, load, arithmetic logic unit (ALU), multiply accumulate unit (MAU) and data select unit (DSU) instruction types are

identified by the letters SLAMD in VIM 109 as follows store (S), load (L), ALU (A), MAU (M), and DSU (D).

The basic concept of loading the iVLIWs is described in further detail in co-pending U.S. Patent Application Serial No. 09/187,539, now U.S. Patent No. 6,151,668, entitled "Methods and Apparatus for Efficient Synchronous MIMD Operations with iVLIW PE-to-PE Communications" and filed November 6, 1998. Also contained in the SP/PE0 and the other PEs is a common PE configurable register file (CRF) 127 which is described in further detail in co-pending U.S. Patent Application Serial No. 09/169,255 entitled "Methods and Apparatus for Dynamic Instruction Controlled Reconfiguration Register File with Extended Precision" filed October 9, 1998. Due to the combined nature of the SP/PE0, the data memory interface controller 125 must handle the data processing needs of both the SP controller, with SP data in memory 121, and PE0, with PE0 data in memory 123. The SP/PE0 controller 125 also is the controlling point of the data that is sent over the 32-bit or 64-bit broadcast data bus 126. The other PEs, 151, 153, and 155 contain common physical data memory units 123', 123'', and 123''' though the data stored in them is generally different as required by the local processing done on each PE. The interface to these PE data memories is also a common design in PEs 1, 2, and 3 and indicated by PE local memory and data bus interface logic 157, 157' and 157''. Interconnecting the PEs for data transfer communications is a cluster switch 171 which is more completely described in co-pending U.S. Patent Application Serial Nos. 08/885,310 entitled "Manifold Array Processor" filed June 30, 1997, now U.S. Patent No. 6,023,753, 08/949,122 entitled "Methods and Apparatus for Manifold Array Processing" filed October 10, 1997, and 09/169,256 entitled "Methods and Apparatus for ManArray PE-to-PE Switch Control" filed October 9, 1998, now U.S. Patent No. 6,167,501. The interface to a host processor, other peripheral devices, and/or external memory can be done in many ways. For completeness, a

primary interface mechanism is contained in a direct memory access (DMA) control unit 181 that provides a scalable ManArray data bus 183 that connects to devices and interface units external to the ManArray core. The DMA control unit 181 provides the data flow and bus arbitration mechanisms needed for these external devices to interface to the ManArray core memories via the multiplexed bus interface symbolically represented by line 185. A high level view of a ManArray control bus (MCB) 191 is also shown in Fig. 1A.--